FIG. 1A
(PRIOR ART)

100

	102 MULTIPLICATION TERMS	=	104 CALCULATION RESULTS FOR p = 11101 & q = 10111	106 CALCULATION RESULTS FOR p = 11101 & q = 10010
107	S(0)	=	000000000	000000000
	q_4*p*x^4	=	111010000 (131)	111010000 (132)
108	$q_4*p*x^4 + S(0) = S(1)$	=	111010000	111010000
	q_3*p*x^3	=	000000000 (127)	000000000 (128)
109	$q_3*p*x^3 + S(1) = S(2)$	=	111010000	111010000
	q_2*p*x^2	=	001110100 (123)	000000000 (124)
110	$q_2*p*x^2 + S(2) = S(3)$	=	110100100	111010000
	q_1*p*x	=	000111010 (119)	000111010 (120)
111	$q_1*p*x + S(3) = S(4)$	=	110011110	111101010
	q_0*p*x^0	=	000011101 (115)	000000000 (116)
112	$q_0*p*x^0 + S(4) = S(5)$	=	110000011 (135)	111101010 (136)

FIG. 1B
(PRIOR ART)

150

```
  11101 = p
x 10111 = q
---------
 000011101  115
 000111010  119
 001110100  123
 000000000  127
 111010000  131
---------
 110000011  135
```

FIG. 1C
(PRIOR ART)

170

```
  11101 = p
x 10010 = q
---------
 000000000  116
 000111010  120
 000000000  124
 000000000  128
 111010000  132
---------
 111101010  136
```

FIG. 2
(PRIOR ART)

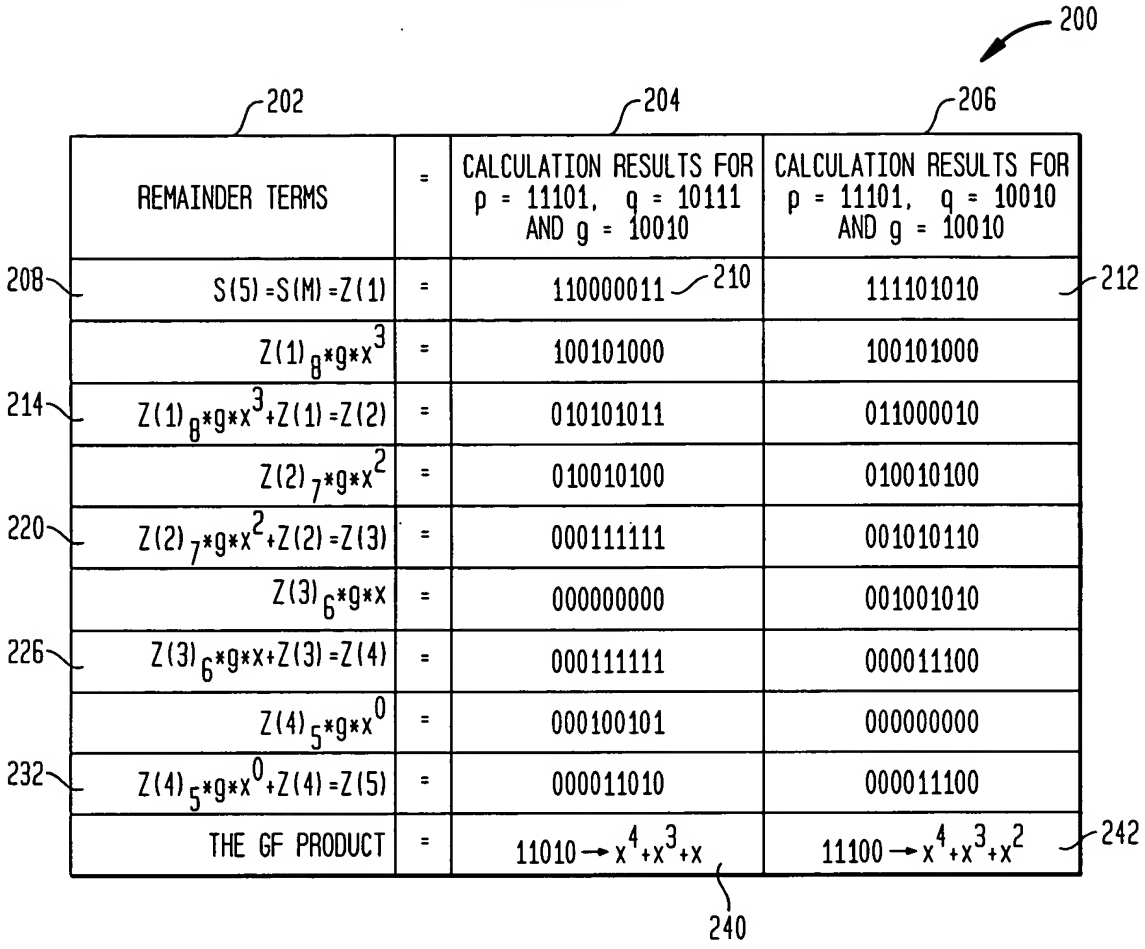

FIG. 3A

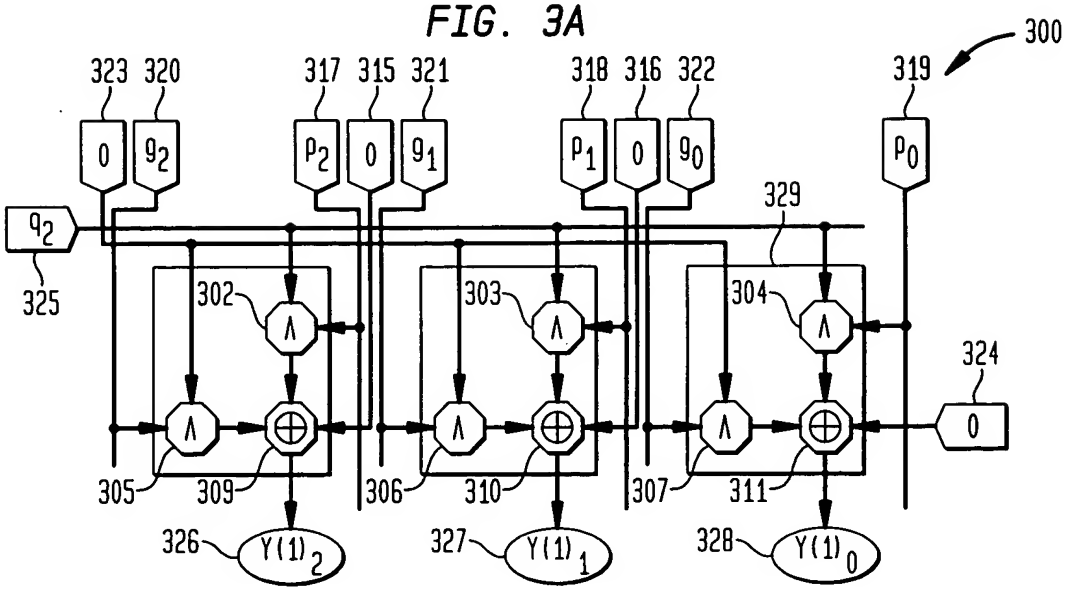
300
323 320
317 315 321
318 316 322
319
0 g2
p2 0 g1
p1 0 g0
p0
329
q2
325
302
303
304
324
0
305 309
306 310
307 311
326 Y(1)2
327 Y(1)1
328 Y(1)0

FIG. 3B

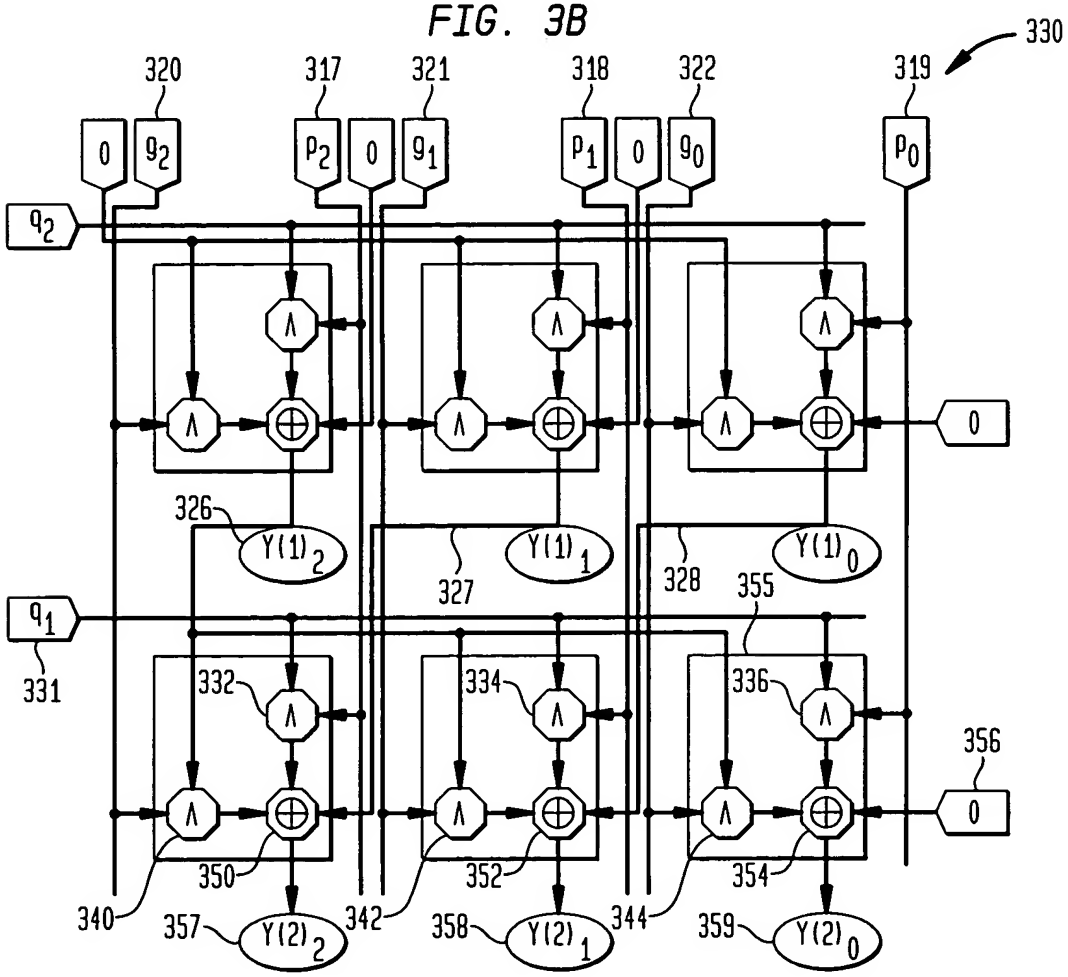
330
320
317 321
318 322
319
0 g2
p2 0 g1
p1 0 g0
p0
q2
0
326 Y(1)2
327 Y(1)1
328 Y(1)0
355
q1
331
332
334
336
356
0
350
352
354
340
342
344
357 Y(2)2
358 Y(2)1
359 Y(2)0

FIG. 3C

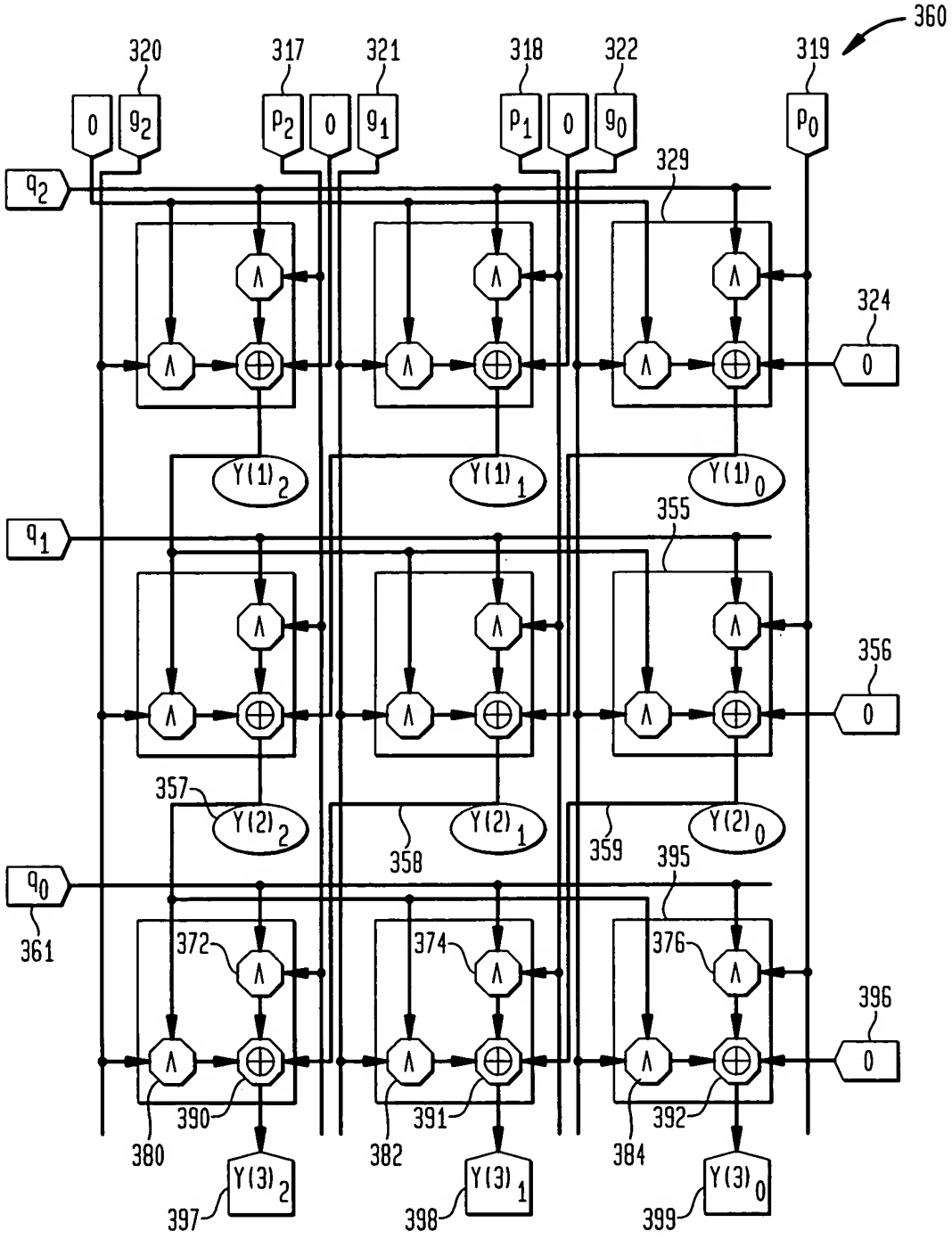
360
320
317
321
318
322
319
0
g2
P2
0
g1
P1
0
g0
P0
329
q2
324
0
Y(1)2
Y(1)1
Y(1)0
355
q1
356
0
357
Y(2)2
Y(2)1
Y(2)0
358
359
395
q0
361
372
374
376
396
0
390
391
392
380
382
384
Y(3)2
Y(3)1
Y(3)0
397
398
399

FIG. 4

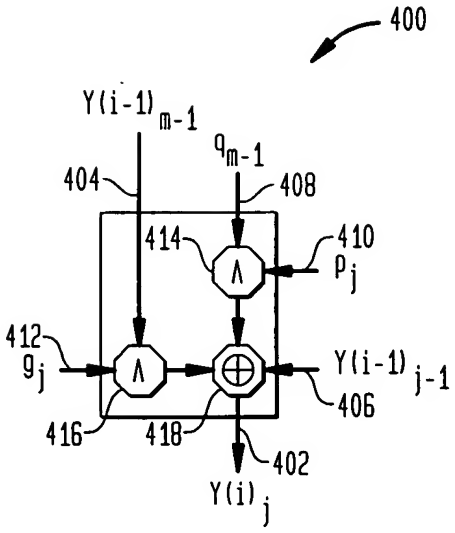
400
Y(i-1)m-1
qm-1
404
408
414
410
pj
412
gj
Y(i-1)j-1
406
416
418
402
Y(i)j

FIG. 5

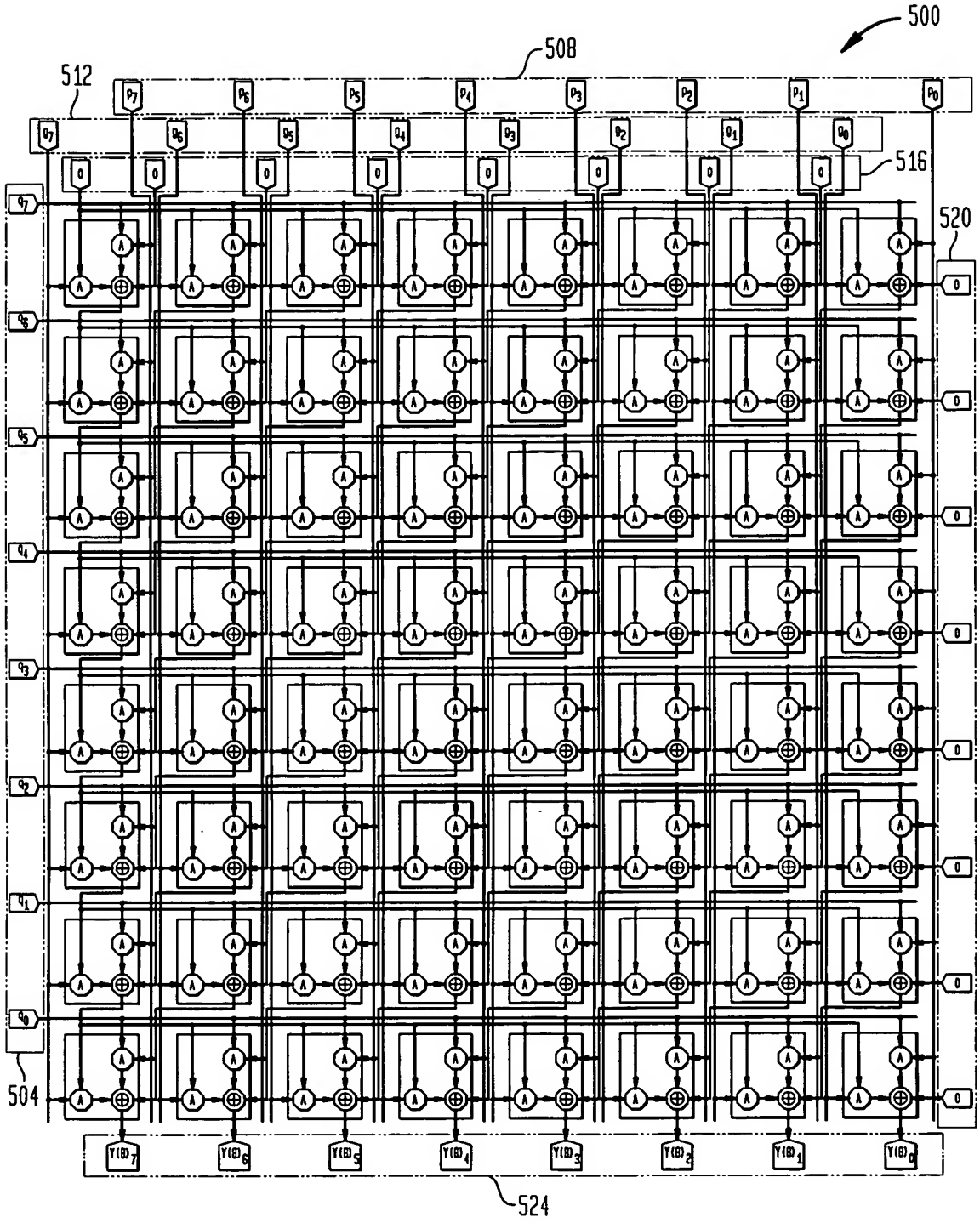

FIG. 6

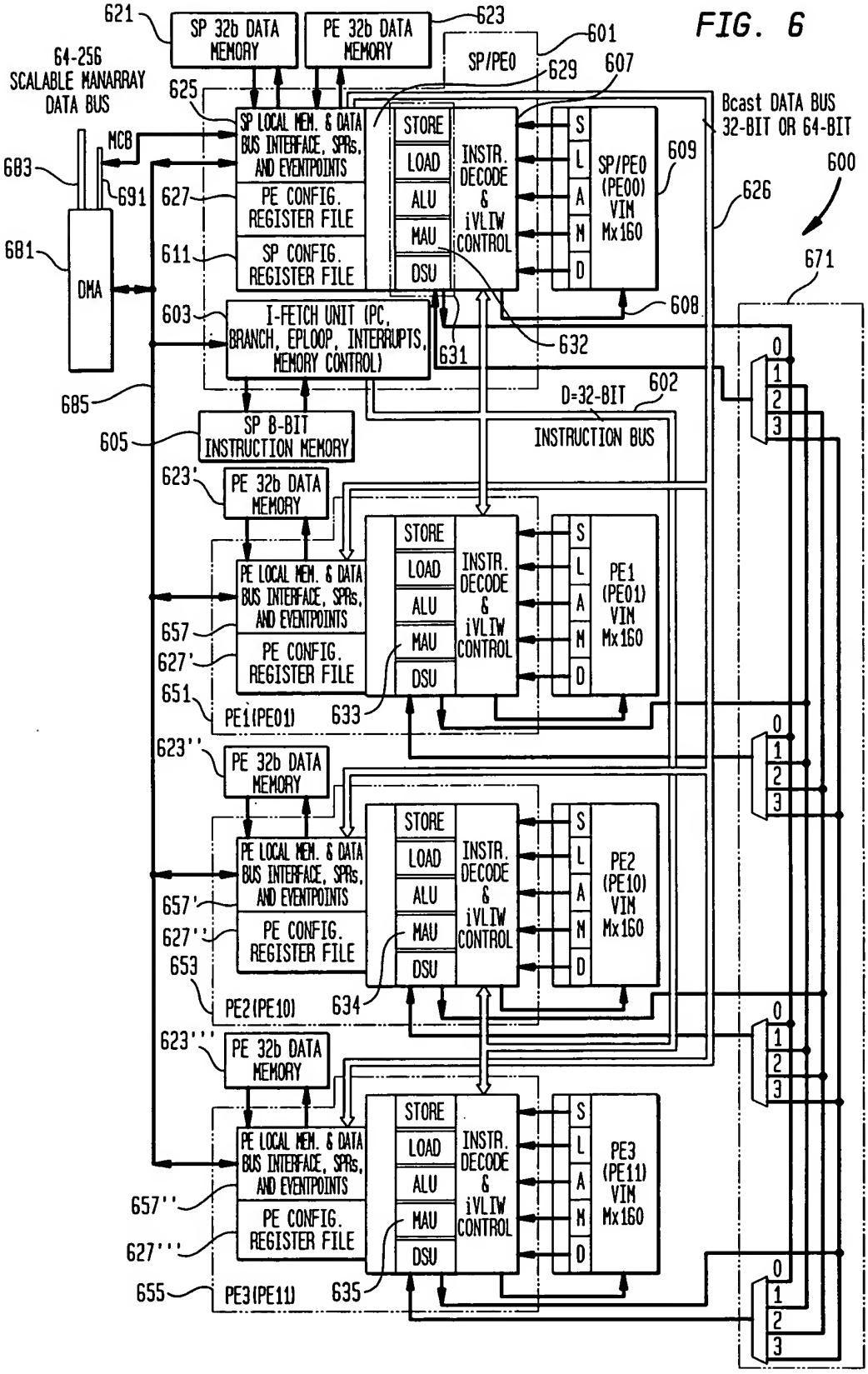
621
SP 32b DATA MEMORY
PE 32b DATA MEMORY
623
601
SP/PE0
629
607
64-256 SCALABLE MANARRAY DATA BUS
625
Bcast DATA BUS 32-BIT OR 64-BIT
600
SP LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 (PE00) VIM Mx160
609
MCB
683
691
627
PE CONFIG. REGISTER FILE
626
681
DMA
611
SP CONFIG. REGISTER FILE
671
603
I-FETCH UNIT (PC, BRANCH, EPLOOP, INTERRUPTS, MEMORY CONTROL)
608
631
632
685
D=32-BIT
602
605
SP 8-BIT INSTRUCTION MEMORY
INSTRUCTION BUS
623'
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
PE1 (PE01) VIM Mx160
657
627'
PE CONFIG. REGISTER FILE
651
PE1(PE01)
633
623''
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
PE2 (PE10) VIM Mx160
657'
627''
PE CONFIG. REGISTER FILE
653
PE2(PE10)
634
623'''
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
PE3 (PE11) VIM Mx160
657''
627'''
PE CONFIG. REGISTER FILE
655
PE3(PE11)
635
0
1
2
3

FIG. 7A

700

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		S/P	Unit		MPYGF opcode						Rt					Rx					Ry					0	CE2		MPack		
											Rte				0	Rxe				0	Rye				0						

FIG. 7B

750

Syntax/Operation

	Instruction	Operands	Operation	ACF
				Quad Bytes
752	MPYGF.[SP]M.4UB	Rt,Rx,Ry	Rt.B3 ←rem(Rx.B3*Ry.B3/PSR.B0 Rt.B2 ←rem(Rx.B2*Ry.B2/PSR.B0 } 757 Rt.B1 ←rem(Rx.B1*Ry.B1/PSR.B0 Rt.B0 ←rem(Rx.B0*Ry.B0/PSR.B0 ~ 755	NONE
752	[TF].MPYGF.[SP]M.4UB	Rt,Rx,Ry	Do operation only if T/F condition is satisfied in F0	NONE
				Octal Bytes
754	MPYGF.[SP]M.8UB	Rte,Rxe,Rye	Rte.B3 ←rem(Rxe.B3*Rye.B3/PSR.B0 Rte.B2 ←rem(Rxe.B2*Rye.B2/PSR.B0 Rte.B1 ←rem(Rxe.B1*Rye.B1/PSR.B0 Rte.B0 ←rem(Rxe.B0*Rye.B0/PSR.B0 Rto.B3 ←rem(Rxo.B3*Ryo.B3/PSR.B0 Rto.B2 ←rem(Rxo.B2*Ryo.B2/PSR.B0 Rto.B1 ←rem(Rxo.B1*Ryo.B1/PSR.B0 Rto.B0 ←rem(Rxo.B0*Ryo.B0/PSR.B0	NONE
754	[TF].MPYGF.[SP]M.8UB	Rte,Rxe,Rye	Do operation only if T/F condition is satisfied in F0	NONE